Features

- Half-bridge SCR configuration integrated in a single package
- High-thermal-conductivity DBC insulation for excellent heat dissipation
- Vacuum soldering technology for enhanced reliability

Product Summary

Applications

- Heating control
- Light control system
- DC motor

Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Parameter	Conditions	Symbol	Values	Unit
Repetitive peak off-state voltage	Tvj = 25°C	V_{DRM}	1600	V
Repetitive peak reverse voltage	Tvj = 25°C	V_{RRM}	1600	V
Non-repetitive peak off-state voltage	Tvj = 25°C	V_{DSM}	1700	V
Non-repetitive peak reverse voltage	Tvj = 25°C	V_{RSM}	1700	V
Average forward current	T_C = 85°C	$I_{T(AV)M}$		

		V_{ISO}	3600/3000	V
Junction temperature range		T_J	-40 ~ +125	
Storage temperature range		T_{stg}	-40 ~ +125	

Electrical Characteristics (@ T_C = 25°C unless otherwise specified)

Parameter	Conditions	Symbol	Values			Unit
			Min.	Typ.	Max.	
Peak forward voltage	I_T=330A, t_P=380μs	V_T			1.80	V
Repetitive peak off-state current	V_D = V_{DRM},T_{vj} = 25	I_{DRM}			100	μA
	V_D = V_{DRM},T_{vj} = 125				40	mA
Reverse leakage current	V_R = V_{RRM},T_{vj} = 25	I_{RRM}			100	μA
	V_R = V_{RRM},T_{vj} = 125				40	mA
Threshold voltage	For power loss calculation only T_{vj} = 125 ,	V_{TO}			0.88	V
Dynamic resistance	T_{vj} = 125 ,	r_T			2.4	mΩ
Triggering gate current	V_D=12V R_L=30Ω	I_{GT}	20		120	mA
Holding current	I_T=1A	I_H			250	mA
Latching current	I_G=1.2 I_{GT}	I_L			300	mA
Critical rate of rise of voltage	V_D=2/3V_{DRM} Tvj=125 Gate Open	dv/dt	1000			V/μs
Triggering gate voltage	V_D=12V R_L=30Ω	V_{GT}			1.8	V
Non triggering gate voltage	V_D=0.5V_{DRM} Tvj=125	V_{GD}	0.25			V

Thermal Characteristics (@ T_C = 25°C unless otherwise specified)

Parameter	Conditions	Symbol	Values			Unit
			Min.	Typ.	Max.	
Thermal resistance, junction to case	per Thyristor	$R_{th(j-c)}$		0		

Ordering Information

Device	Marking	Package	Weight	Inner Box	Pre Carton
JMT110KT16T1	JMT110KT16T1	T1	100g 5/PCS	10 PCS	120 PCS

Typical Electrical & Thermal Characteristics

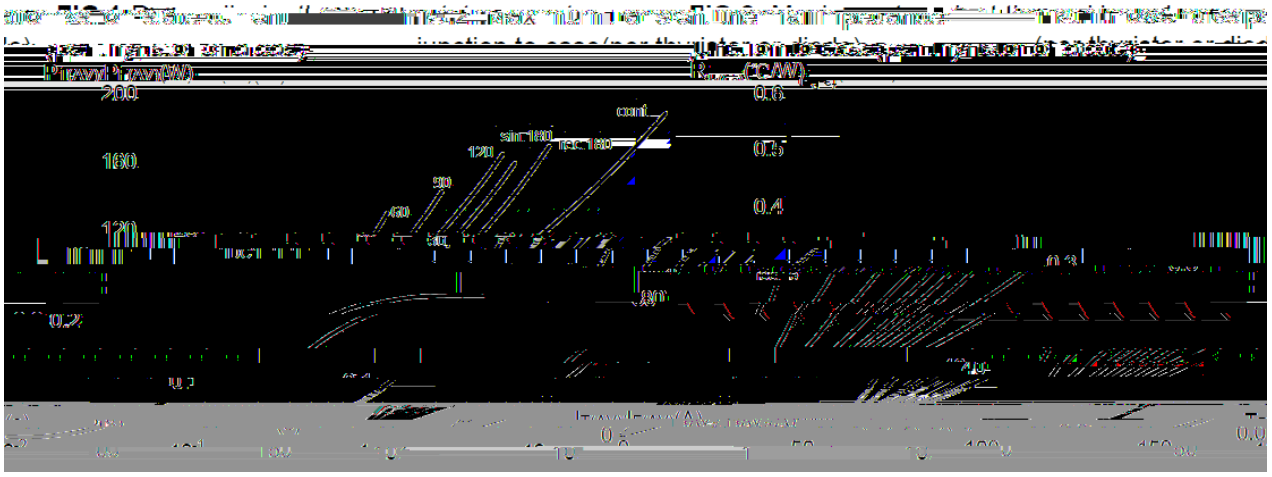

FIG.3:Forward characteristics

FIG.4: Relative variations of gate trigger current, holding

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Semiconductor Co., Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. This information in this document is subject to change without prior notice. Notwithstanding this, Jiangsu JieJie will fully comply with the terms outlined in a signed agreement. Products and information provided in this .178 Tw
[illegible]