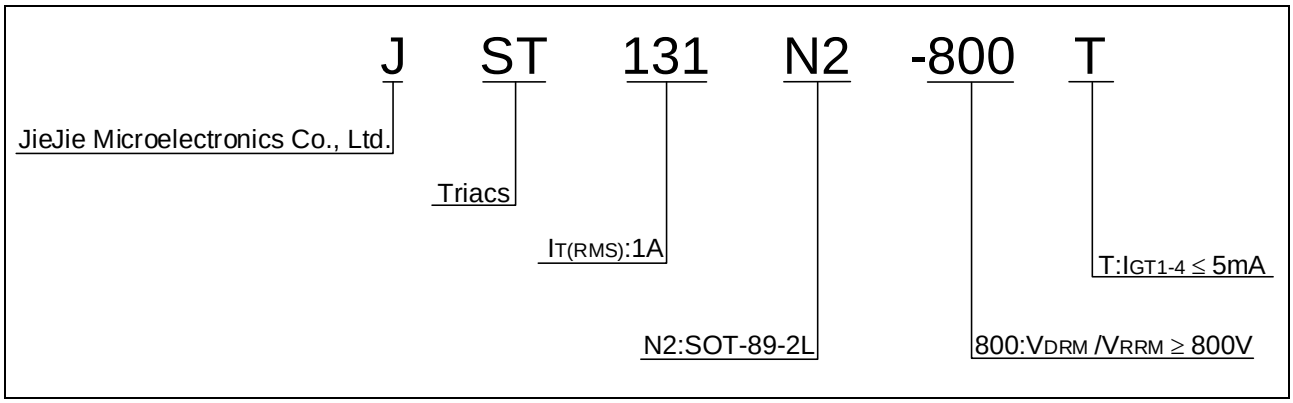
JST131N2-800T 1A TRIAC Rev.A.

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_D=12V R_L=33Ω	ALL	MAX.	5	mA
V_{GT}		ALL	MAX.	1.3	V
V_{GD}	V_D=V_{DRM} T_j=125 R_L=3.3kΩ	ALL	MIN.	0.2	V
I_L	I_G=1.2I_{GT}	- -	MAX.	5	mA
				10	
I_H	I_T=50mA		MAX.	5	mA
dV/dt	V_D=540V Gate Open T_j=110		MIN.	20	V/μs
(dV/dt)c	(dI/dt)c=0.44A/ms, T_j=110		MIN.	1	V/μs
t_{on}	I_G=10mA I_A=200mA I_R=20mA T_j=25		TYP.	2	μs
t_{off}				20	

Symbol	Parameter		Value(MAX.)	Unit
V_{TM}	I_{TM}=1.4A t_p=380μs	T_j=25	1.45	V
V_{TO}	Threshold voltage	T_j=125	0.96	V
R_D	Dynamic resistance	T_j=125	225	mΩ
I_{DRM}	V_D=V_{DRM} V_R=V_{RRM}	T_j=25	5	μA
I_{RRM}		T_j=125	0.25	mA

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	junction to case (AC)	50	/W
$R_{th(j-a)}$	junction to ambient (AC, in free air, S=5cm^2)	100	/W


J
ST
131
N2
-800
T
JieJie Microelectronics Co., Ltd.
Triacs
IT(RMS):1A
N2:SOT-89-2L
800:VDRM /VRRM ≥ 800V
T:IGT1-4 ≤ 5mA

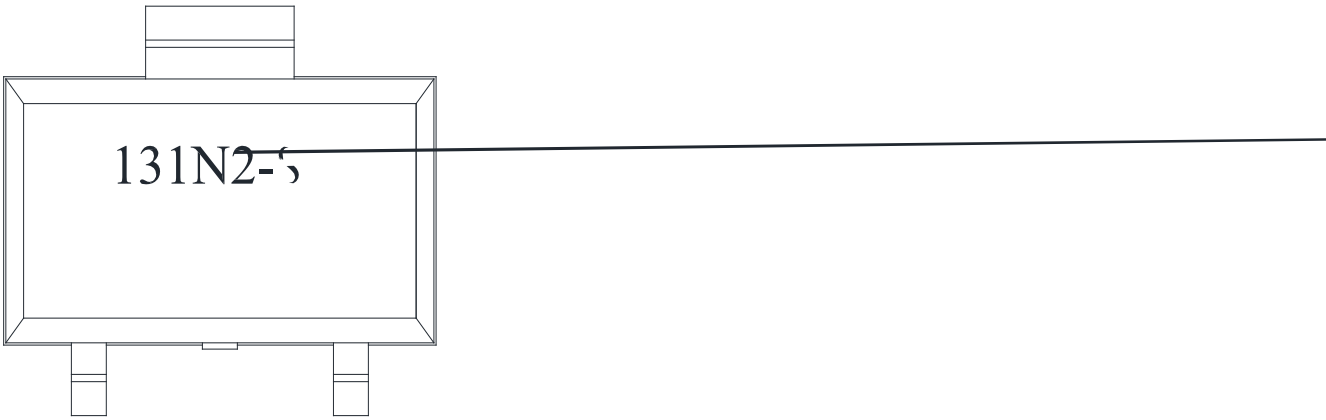
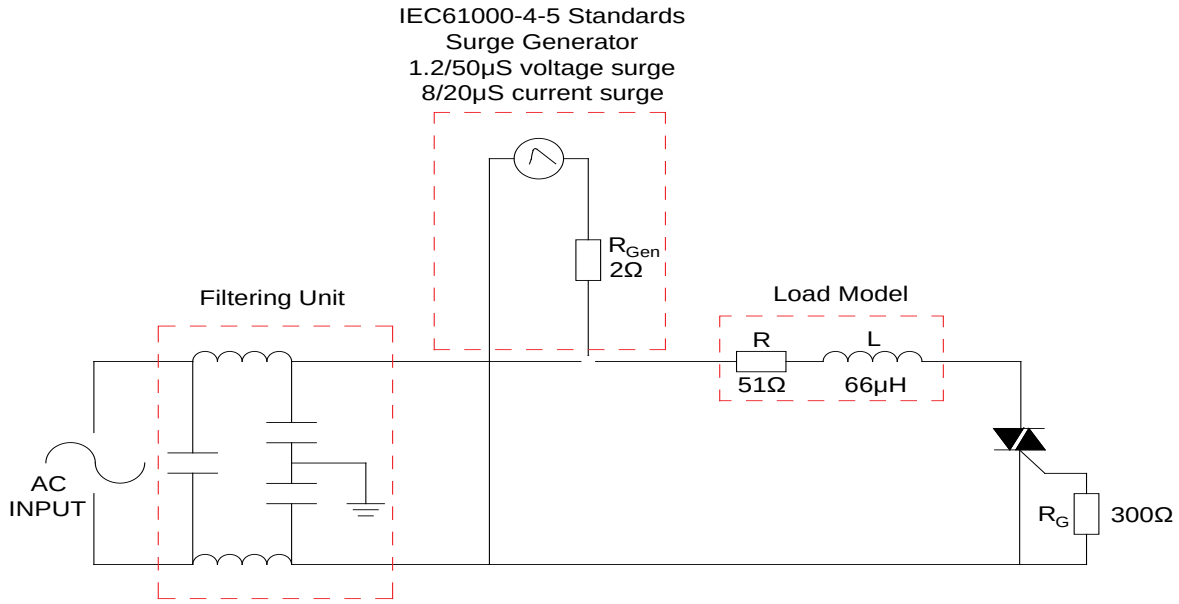

131N2-S

FIG.1: Maximum power dissipation versus RMS on-state current

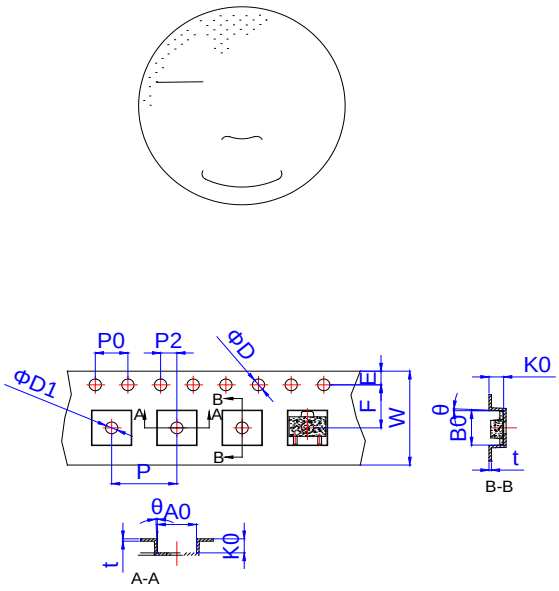
FIG.2: RMS on-state current versus case temperature 278550 -0.4529062 0 0.0009766 cm 0.831 s

FIG.7: Relative variations of gate trigger current, holding current and latching current versus junction temperature 1

FIG.8 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



Order code	Voltage V



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E	1.65	1.75	1.85	0.065	0.069	0.073
F	5.45	5.50	5.55	0.215	0.217	0.219
P2	1.90	2.00	2.10	0.075	0.079	0.082
D	-	1.50	1.60	-	0.059	0.063
D1	1.50	-	-	0.059	-	-
P0	3.90	4.00	4.10	0.154	0.157	0.161
10P0	39.80	40.00	40.20	1.567	1.575	1.583
W	-	-	12.30	-	-	0.482
P	7.90	8.00	8.10	0.311	0.315	0.319
A0	5.20	5.30	5.40	0.204	0.208	0.212
B0	4.80	4.90	5.00	0.188	0.192	0.196
K0	1.75	1.85	1.95	0.069	0.073	0.076
t	0.20	0.25	0.30	0.008	0.010	0.012
θ	3°		5°	3°		5°

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