



Peak gate current ($t_p=20\mu s$, $T_j=125$)	I_{GM}	4	A
Average gate power dissipation ($T_j=125$)	$P_{G(AV)}$	0.5	W
Peak gate power	P_{GM}	10	W
Peak pulse voltage ($T_j=25$; non-repetitive, off-state; FIG.7)	V_{pp}	3.5	kV

(T_j=25 unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	$V_D=12V$ $R_L=33\Omega$	- -	MAX.	5	mA
V_{GT}		- -	MAX.	1	V
V_{GD}	$V_D=V_{DRM}$ $T_j=125$ $R_L=3.3k\Omega$	- -	MIN.	0.2	V
I_L	$I_G=1.2I_{GT}$	-	MAX.	10	mA
				15	
I_H	$I_T=100mA$		MAX.	10	mA
dV/dt	$V_D=400V$ Gate Open $T_j=125$		MIN.	150	V/ μs
(dI/dt) _c	(dV/dt) _c =10V/ μs , $T_j=125$		MIN.	0.5	A/ms
t_{on}	$I_G=10mA$ $I_A=200mA$ $I_R=20mA$ $T_j=25$		TYP.	2	μs
t_{off}				20	

Symbol	Parameter		Value(MAX.)	Unit
V_{TM}	$I_{TM}=8.5A$ $t_p=380\mu s$	$T_j=25$	1.5	V
V_{TO}	Threshold voltage	$T_j=125$	0.82	V
R_D	Dynamic resistance	$T_j=125$	57	m Ω
I_{DRM}	$V_D=V_{DRM}$ $V_R=V_{RRM}$	$T_j=25$	5	μA
I_{RRM}		$T_j=125$	0.2	mA

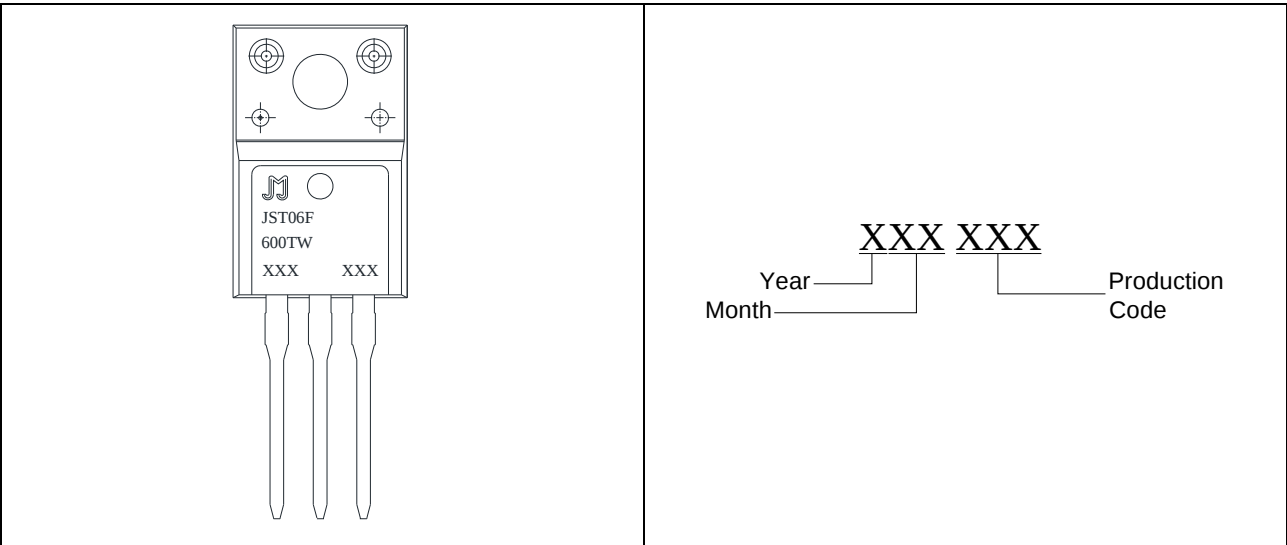
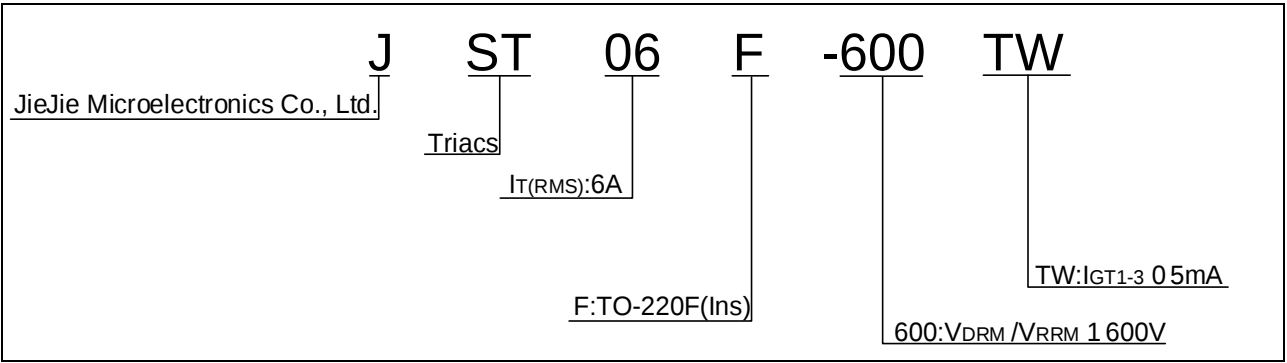
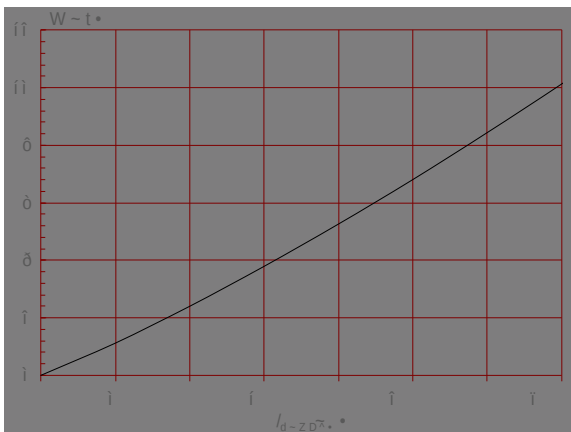
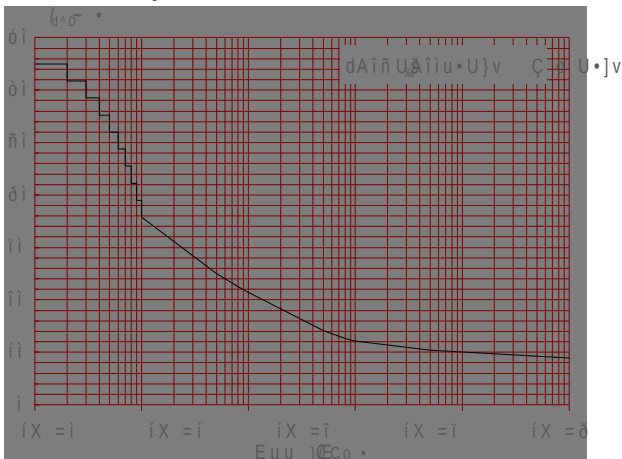
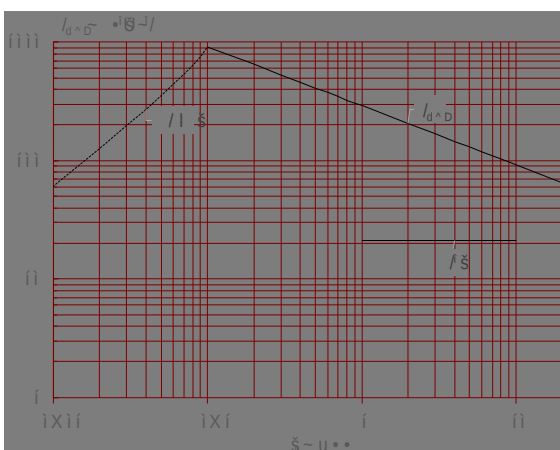
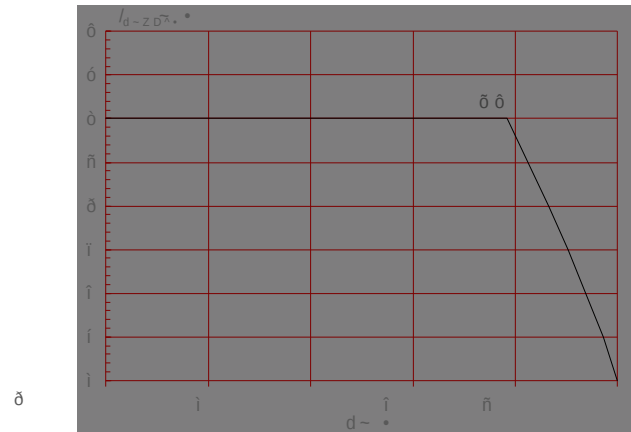
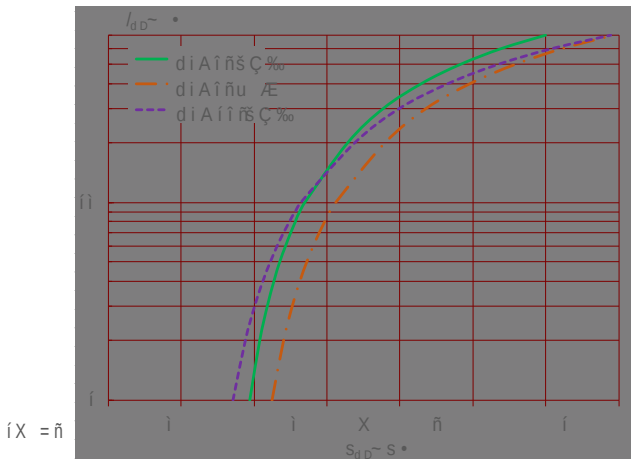


FIG.1: Maximum power dissipation versus RMS on-state current**FIG.3:** Surge peak on-state current versus number of cycles**FIG.5:** Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of I^2t ($dI/dt < 100\text{A}/\mu\text{s}$)**FIG.2:** RMS on-state current versus case temperature**FIG.4:** On-state characteristics**FIG.6:** Relative variations of gate trigger current, holding current and latching current versus junction temperature



Order code	Voltage V _{DRM} /V _{RRM} (V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
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