

Average gate power dissipation ($T_j=150$)	$P_{G(AV)}$	1	W
Peak gate power	P_{GM}	22	W
Peak pulse voltage ($T_j=25$; non-repetitive,off-state;FIG.7)	V_{pp}	1	kV

($T_j=25$)

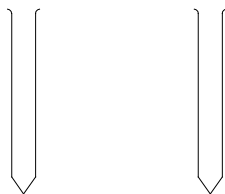
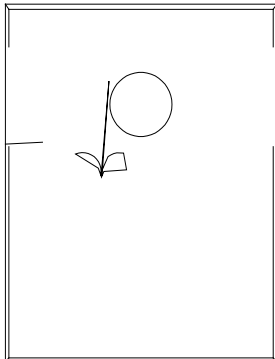
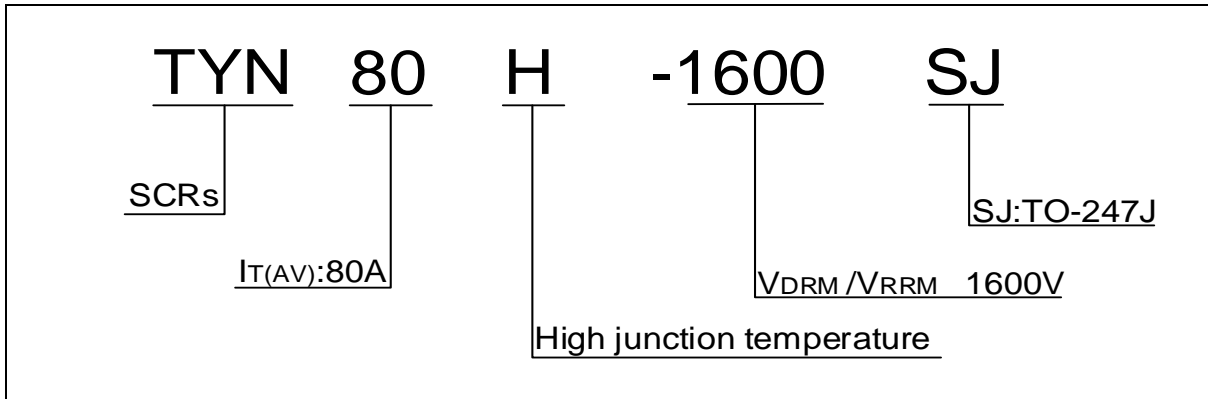
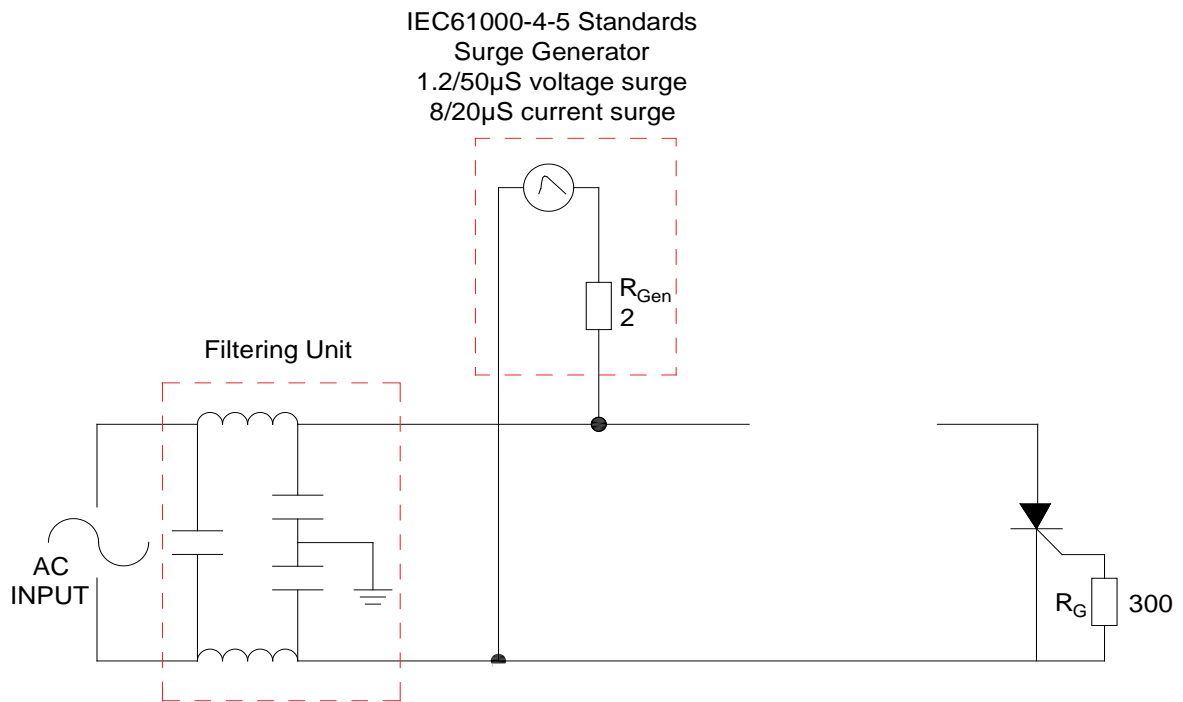
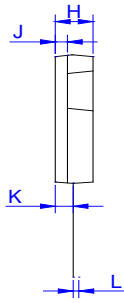
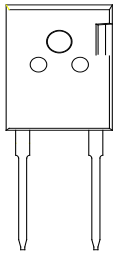


FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards.




Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(mA)	
------------	----------------------------------	---------	--



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.50		16.10	0.610		0.634
B1	3.10		3.50	0.122		0.138
C	19.70		20.30	0.776		0.799
D	2.90		3.30	0.114		0.130
E	1.90		2.30	0.075		0.091
F	1.00		1.40	0.039		0.055
G		5.44			0.214	

H	4.80	5.20	0.189	0.205
J	1.90	2.10	0.075	0.083
K	2.20	2.50	0.087	0.098
L	0.41	0.79	0.016	0.031

Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement. Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.

 is a registered trademark of Jiangsu JieJie Microelectronics Co., Ltd. Copyright © 2025 Jiangsu JieJie Microelectronics Co., Ltd. All rights reserved.