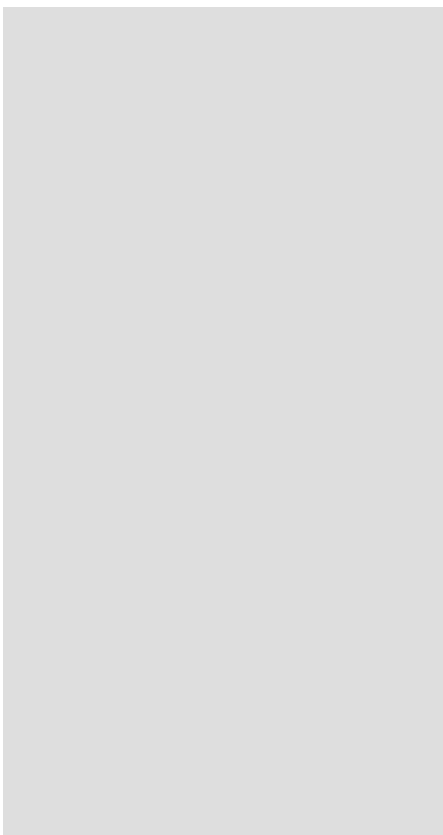






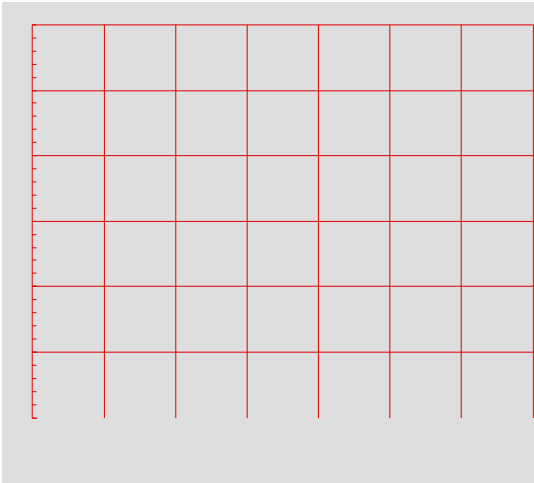
Average gate power dissipation ($T_j=125^\circ\text{C}$)	$P_{G(AV)}$	0.5	W
Peak gate power	P_{GM}	10	W
Peak pulse voltage ($T_j=25^\circ\text{C}$; non-repetitive, off-state; FIG. 7)	V_{pp}	3.5	kV

ELECTRICAL CHARACTERISTICS ($T_j=25^\circ\text{C}$ unless otherwise specified)

I_{GT}	$V_D=12\text{V } R_L=33\Omega$	- -	MAX.	10	mA
V_{GT}		- -	MAX.	1	V
V_{GD}	$V_D=V_{DRM} T_j=125^\circ\text{C}$ $R_L=3.3\text{k}\Omega$	- -	MIN.	0.2	V
I_L	$I_G=1.2I_{GT}$	-	MAX.	20	mA
				35	
I_H	$I_T=100\text{mA}$		MAX.	20	mA
dV/dt	$V_D=540\text{V}$ Gate Open $T_j=125^\circ\text{C}$		MIN.	500	



Maximum power dissipation versus RMS
on-state current



RMS on-state current versus case
temperature



FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards





Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.

 is a registered trademark of Jiangsu JieJie Microelectronics Co., Ltd.
Copyright © 2025 Jiangsu JieJie Microelectronics Co., Ltd. All rights reserved.